a plurality of patterned circuit layer;

at least an insulative layer stacked between the patterned circuit layers for isolating the patterned circuit layers, and the patterned circuit layers are electrically connected one another, and one of the patterned circuit layer is positioned on the surface of the substrate of the flip chip package, and the patterned circuit layer comprises at least a plurality of a first mounting pad and a plurality of a second mounting pad; and

a solder mask layer covering the patterned circuit layer on the surface of the substrate of the flip chip package, a portion of the surface on the outer edge of the first mounting pad and a side surface of the first mounting pad while exposing a portion of the surface of the first mounting pad and the whole surface of the second mounting pad, wherein the first mounting pads are disposed on the peripheral region of the substrate and the second mounting pads are disposed at a central region of the substrate.

Subt B3

7. (Once Amended) A substrate structure of Flip Chip package comprising:

a plurality of patterned circuit layer;

at least an insulative layer stacked between the patterned circuit layers for isolating the patterned circuit layers, and the patterned circuit layers are electrically connected one another, and one of the patterned circuit layer is positioned on the surface of the substrate of the flip chip package, and the patterned circuit layer comprises at least a plurality of a first mounting pad and a plurality of a second mounting pad;

a solder mask layer covering the patterned circuit layer on the surface of the substrate of the flip chip package and a portion of the surface on the outer edge of the first mounting pad while exposing a portion of the surface of the first mounting pad and the whole surface of the

second mounting pad, wherein the first mounting pads are formed at the peripheral region of the substrate;

a chip having an active surface with a plurality of bumps disposed thereon wherein the chip has its active surface face to the surface of the substrate of the flip chip package, and the bumps are electrically connected to their corresponding first bonding pads and second bonding pads respectively; and

an underfill material filling between the active surface of the chip and the top surface of the substrate of the flip chip package.

12. (Once Amended) The substrate structure of Flip Chip package of claim 7 wherein the second mounting pads are disposed in the central region of the substrate of the flip chip package.

Present Status of the Application

Claims 1, 5-7 and 11-13 are rejected under 35 USC 103 (a) as being unpatentable over Lach et al. (U. S. Patent No. 6,108,212).

Claims 2-4, 8-10 and 14 are rejected under 35 USC 103 (a) as being unpatentable over Lach et al. (U. S. Patent No. 6,108,212) in view of Admitted Prior Art (APA).

Claims 4 and 10 are rejected under 35 USC 103 (a) as being unpatentable over Lach et al. (U. S. Patent No. 6,108,212) and APA further in view of Katchmar (U. S. Patent No. 6,194,782) .

REMARK

Claims 1-14 are presently pending, of which claims 1,7 and 12 have been amended and claim 6 is cancelled for the purpose of clarification. No new matter has been added to the